RENESAS

DATASHEET

ICL7106, ICL7107, ICL7107S

3 1/2 Digit, LCD/LED Display, A/D Converters

FN3082
Rev 9.00
October 24, 2014

The Intersil ICL7106 and ICL7107 are high performance, low power, $3^1/_2$ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7106 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the ICL7107 will directly drive an instrument size light emitting diode (LED) display.

The ICL7106 and ICL7107 bring together a combination of high accuracy, versatility, and true economy. It features auto zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA (max) and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation (ICL7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

Features

- Guaranteed zero reading for 0V input on all scales
- True polarity at zero for precise null detection
- 1pA typical input current
- True differential input and reference, direct display drive
  - LCD ICL7106, LED ICL7107
- Low noise - less than $15\mu V_{P-P}$
- On-chip clock and reference
- Low power dissipation - typically less than 10mW
- No additional active circuits required
- Enhanced display stability
- Pb-free (RoHS compliant)

Ordering Information

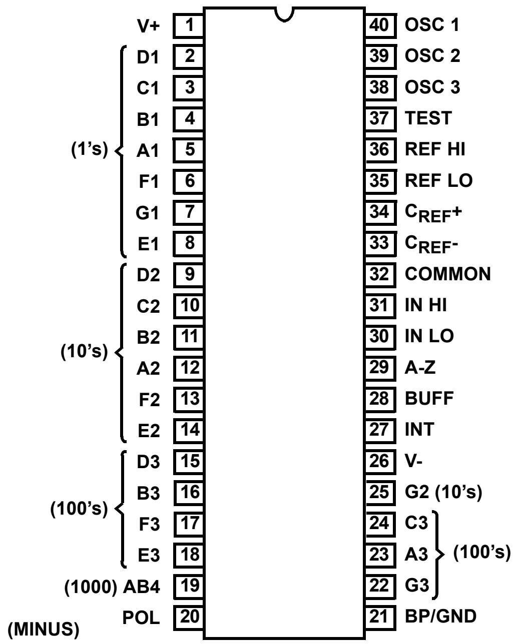
PART NUMBER (Note 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ICL7106CPLZ	ICL7106CPLZ	0 to 70	40 Ld PDIP (Note 3)	E40.6
ICL7106CM44Z (Note 4)	ICL7106 CM44Z	0 to 70	44 Ld MQFP	Q44.10x10
ICL7106CM44ZT (Notes 4, 5)	ICL7106 CM44Z	0 to 70	44 Ld MQFP Tape and Reel	Q44.10x10
ICL7107CPLZ	ICL7107CPLZ	0 to 70	40 Ld PDIP (Note 3)	E40.6
ICL7107SCPLZ	ICL7107SCPLZ	0 to 70	40 Ld PDIP (Notes 1, 3)	E40.6
ICL7107CM44Z (Note 4)	ICL7107 CM44Z	0 to 70	44 Ld MQFP	Q44.10x10
ICL7107CM44ZT (Notes 4, 5)	ICL7107 CM44Z	0 to 70	44 Ld MQFP Tape and Reel	Q44.10x10

NOTES:

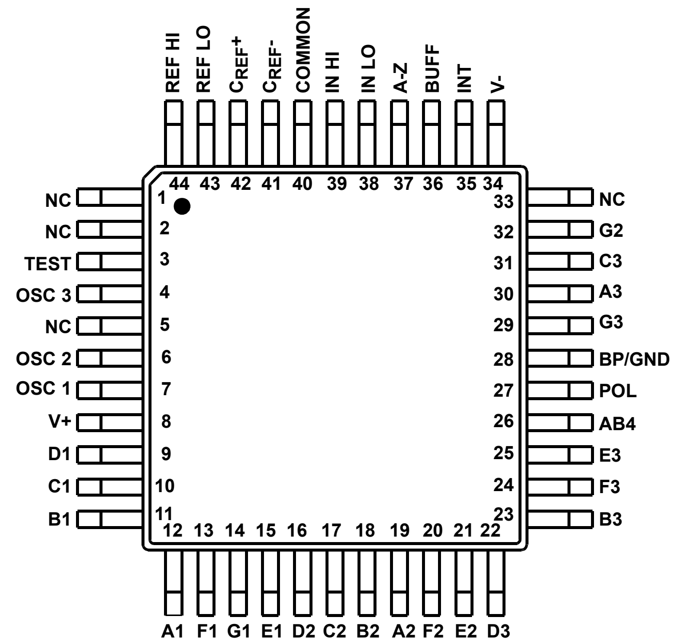
1. “S” indicates enhanced stability.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
4. For Moisture Sensitivity Level (MSL), please see product information page for ICL7106, ICL7107, ICL7107S. For more information on MSL, please see tech brief TB363.
5. Please refer to TB347 for details on reel specifications.

Pin Configurations

ICL7106, ICL7107, ICL7107S (PDIP)
TOP VIEW



ICL7106, ICL7107 (MQFP)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage
- ICL7106, V+ to V- 15V
- ICL7107, V+ to GND 6V
- ICL7107, V- to GND. . . . . -9V

Analog Input Voltage (Either Input) (Note 6) . . . . V+ to V-
Reference Input Voltage (Either Input). . . . . V+ to V-
Clock Input
- ICL7106 . . . . TEST to V+
- ICL7107 . . . . GND to V+

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
PDIP Package (Note 7)	50
MQFP Package (Note 7)	75

Maximum Junction Temperature . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile (MQFP Package only) . . . . see TB493

NOTE: Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Operating Conditions

Temperature Range . . . . 0°C to +70°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
7. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications (Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Zero Input Reading	V_{IN} = 0.0V, full scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Stability (Last Digit) (ICL7107S Only)	Fixed input voltage (Note 11)	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error	$-V_{IN}$ = $+V_{IN}$ ≅ 200mV Difference in reading for equal positive and negative inputs near full scale	-	±0.2	±1	Counts
Linearity	Full scale = 200mV or full scale = 2V maximum deviation from best straight line fit (Note 10)	-	±0.2	±1	Counts
Common Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, full scale = 200mV (Note 10)	-	50	-	µV/V
Noise	V_{IN} = 0V, full scale = 200mV (peak-to-peak value not exceeded 95% of time)	-	15	-	µV
Leakage Current Input	V_{IN} = 0 (Note 10)	-	1	10	pA
Zero Reading Drift	V_{IN} = 0, 0°C to +70°C (Note 10)	-	0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0°C to +70°C, (ext. ref. 0ppm/×°C) (Note 10)	-	1	5	ppm/°C
End Power Supply Character V+ Supply Current	V_{IN} = 0 (does not include LED current for ICL7107)	-	1.0	1.8	mA
End Power Supply Character V- Supply Current	ICL7107 Only	-	0.6	1.8	mA
COMMON Pin Analog Common Voltage	25kΩ between common and positive supply (with respect to + supply)	2.4	3.0	3.2	V
Temperature Coefficient of Analog Common	25kΩ between common and positive supply (with respect to + supply)	-	80	-	ppm/°C
DISPLAY DRIVER ICL7106 ONLY					
Peak-to-Peak Segment Drive Voltage Peak-to-Peak Backplane Drive Voltage	V+ = to V- = 9V (Note 9)	4	5.5	6	V

Electrical Specifications (Note 8) (Continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISPLAY DRIVER ICL7107 ONLY						
Segment Sinking Current		V+ = 5V, segment voltage = 3V				
	Except Pins AB4 and POL		5	8	-	mA
	Pin AB4 Only		10	16	-	mA
	Pin POL Only		4	7	-	mA

NOTES:

8. Unless otherwise noted, specifications apply to both the ICL7106 and ICL7107 at T_A = +25°C, f_{CLOCK} = 48kHz. ICL7106 is tested in the circuit of Figure 1. ICL7107 is tested in the circuit of Figure 2.
9. Back plane drive is in phase with segment drive for “off” segment, 180 degrees out of phase for “on” segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
10. Limit is not production tested. The maximum was established via characterization and/or design simulations.
11. Sample tested.

Typical Applications and Test Circuits

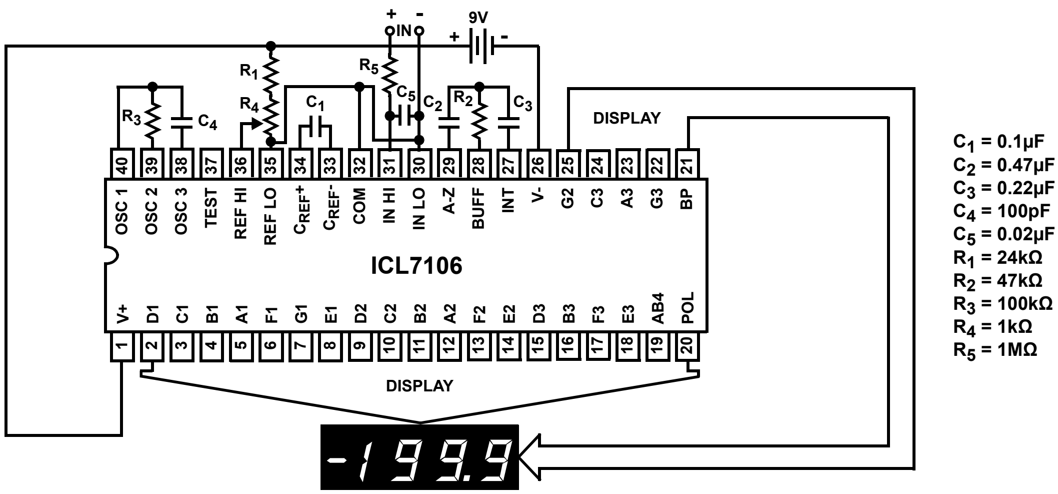


FIGURE 1. ICL7106 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

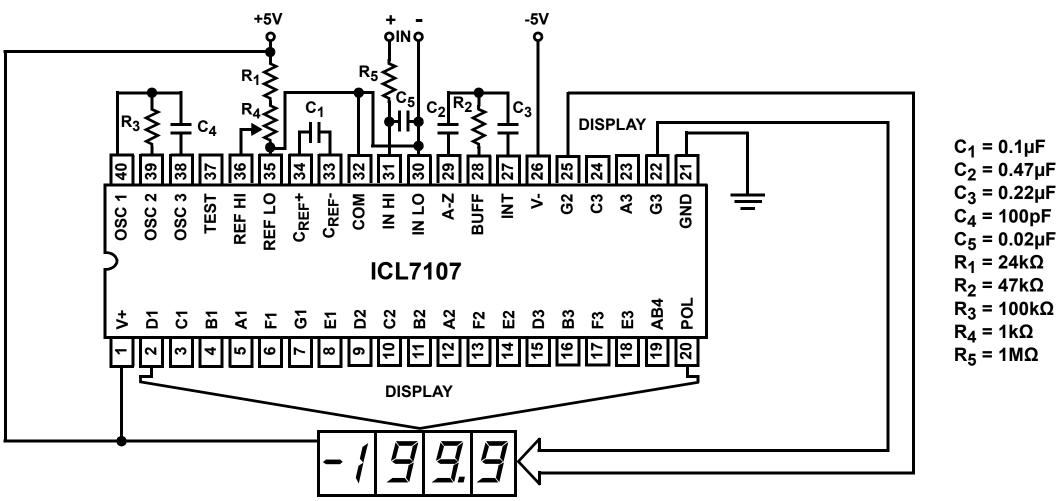


FIGURE 2. ICL7107 TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50k\Omega$
  f_{OSC} (Typ) = 48kHz

- **OSCILLATOR PERIOD**

  $t_{OSC} = RC/0.45$

- **INTEGRATION CLOCK FREQUENCY**

  $f_{CLOCK} = f_{OSC}/4$

- **INTEGRATION PERIOD**

  $t_{INT} = 1000 \times (4/f_{OSC})$

- **60/50Hz REJECTION CRITERION**

  t_{INT}/t_{60Hz} or t_{INT}/t_{60Hz} = Integer

- **OPTIMUM INTEGRATION CURRENT**

  $I_{INT} = 4\mu A$

- **FULL SCALE ANALOG INPUT VOLTAGE**

  V_{INFS} (Typ) = 200mV or 2V

- **INTEGRATE RESISTOR**

  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

  $$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

  $$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

- **V_{INT} MAXIMUM SWING:**

  $(V- + 0.5V) < V_{INT} < (V+ - 0.5V)$, V_{INT} (Typ) = 2V

- **DISPLAY COUNT**

  $$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**

  $t_{CYC} = t_{CLOCK} \times 4000$
  $t_{CYC} = t_{OSC} \times 16,000$
  when f_{OSC} = 48kHz; t_{CYC} = 333ms

- **COMMON MODE INPUT VOLTAGE**

  $(V- + 1V) < V_{IN} < (V+ - 0.5V)$

- **AUTO-ZERO CAPACITOR**

  $0.01\mu F < C_{AZ} < 1\mu F$

- **REFERENCE CAPACITOR**

  $0.1\mu F < C_{REF} < 1\mu F$

- **V_{COM}**

  Biased between Vi and V-.

- **$V_{COM} \cong V+ - 2.8V$**

  Regulation lost when V+ to V- < ≅6.8V
  If V_{COM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

- **ICL7106 POWER SUPPLY: SINGLE 9V**

  V+ - V- = 9V
  Digital supply is generated internally
  $V_{GND} \cong V+ - 4.5V$

- **ICL7106 DISPLAY: LCD**

  Type: Direct drive with digital logic supply amplitude.

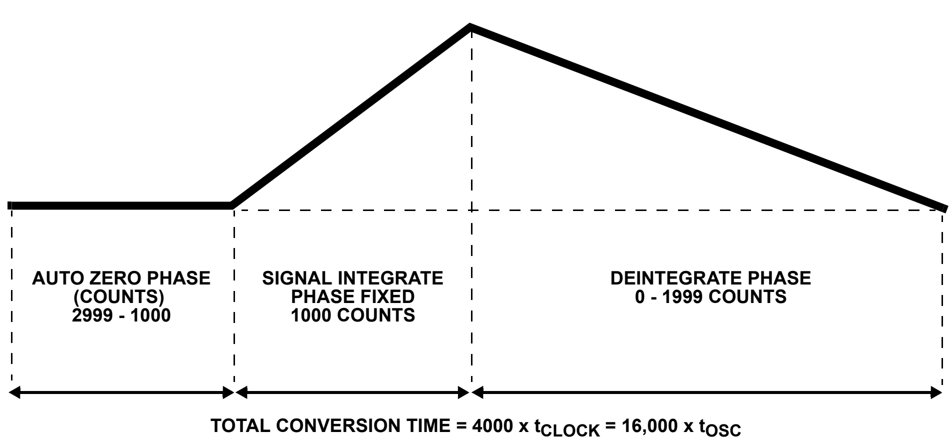
- **ICL7107 POWER SUPPLY: DUAL ±5.0V**

  V+ = +5V to GND
  V- = -5V to GND
  Digital Logic and LED driver supply V+ to GND

- **ICL7107 DISPLAY: LED**

  Type: Nonmultiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



Detailed Description

Analog Section

Figure 3 shows the analog section for the ICL7106 and ICL7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Deintegrate Phase

The final phase is deintegrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000\left(\frac{V_{IN}}{V_{REF}}\right) \quad \text{(EQ. 1)}$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (see "Component Value Selection" on page 10.)

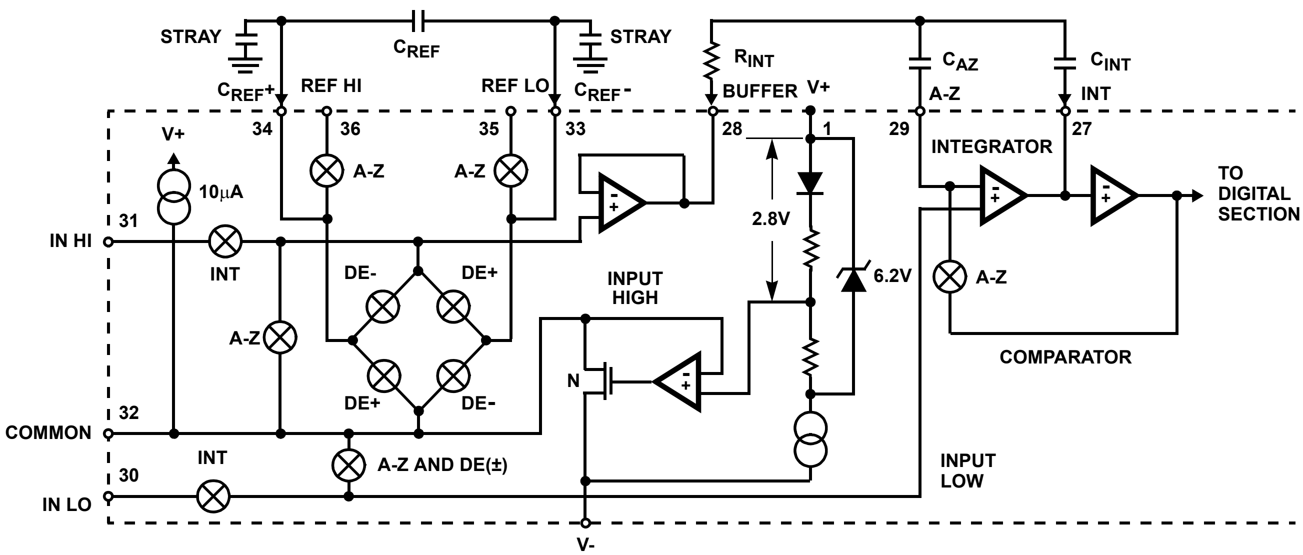


FIGURE 3. ANALOG SECTION OF ICL7106 AND ICL7107

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (ICL7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/×°C.

The limitations of the on chip reference should also be recognized, however. With the ICL7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25μV to $80\mu V_{P-P}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overrange and a non-overrange count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The ICL7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and deintegrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

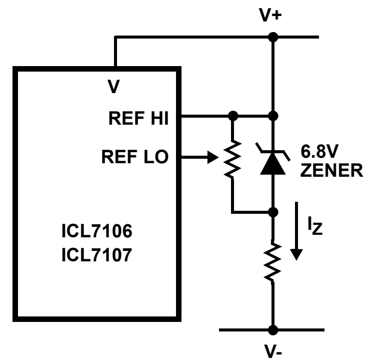


FIGURE 4A.

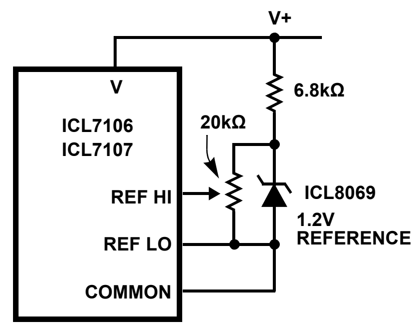


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the ICL7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

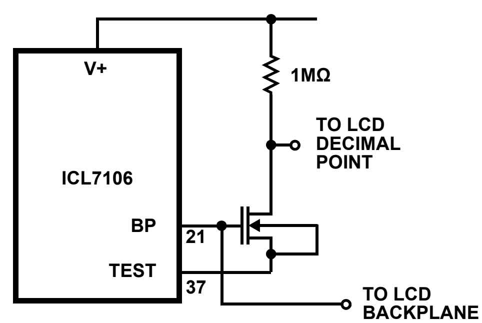


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

The second function is a “lamp test”. When TEST is pulled high (to V+) all segments will be turned on and the display should read “1888”. The TEST pin will sink about 15mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

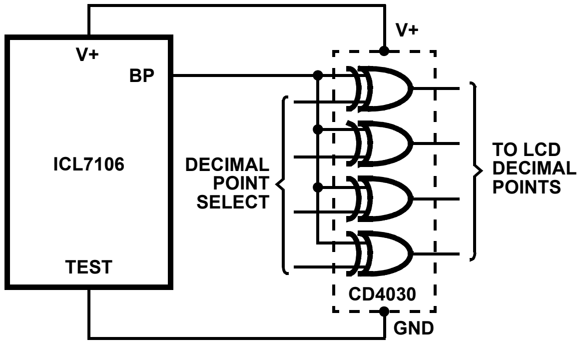


FIGURE 6. EXCLUSIVE ‘OR’ GATE FOR DECIMAL POINT DRIVE

Digital Section

Figures 7 and 8 show the digital section for the ICL7106 and ICL7107, respectively. In the ICL7106, an internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/sec., this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the ICL7107. It is identical to the ICL7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is “on” for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

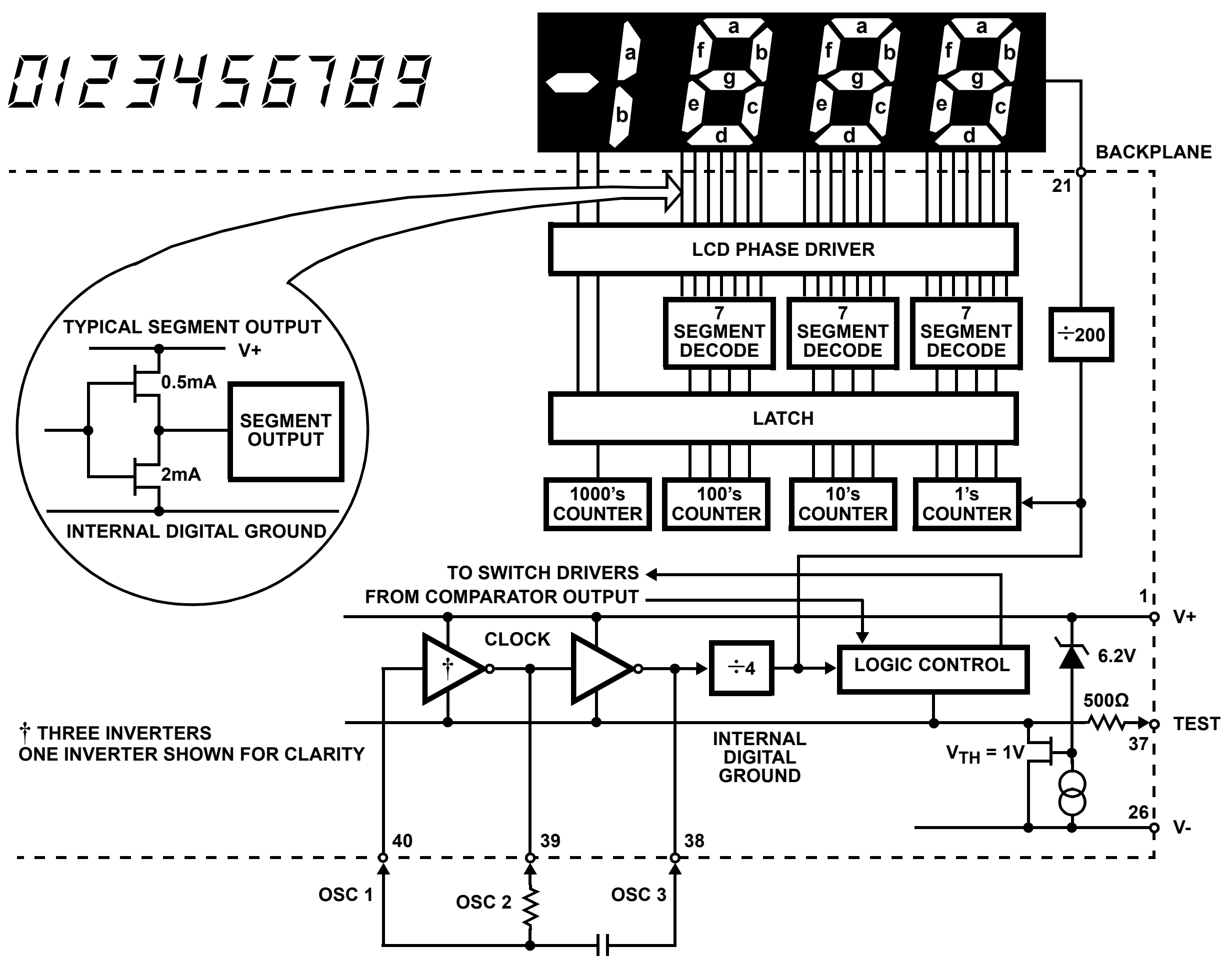


FIGURE 7. ICL7106 DIGITAL SECTION

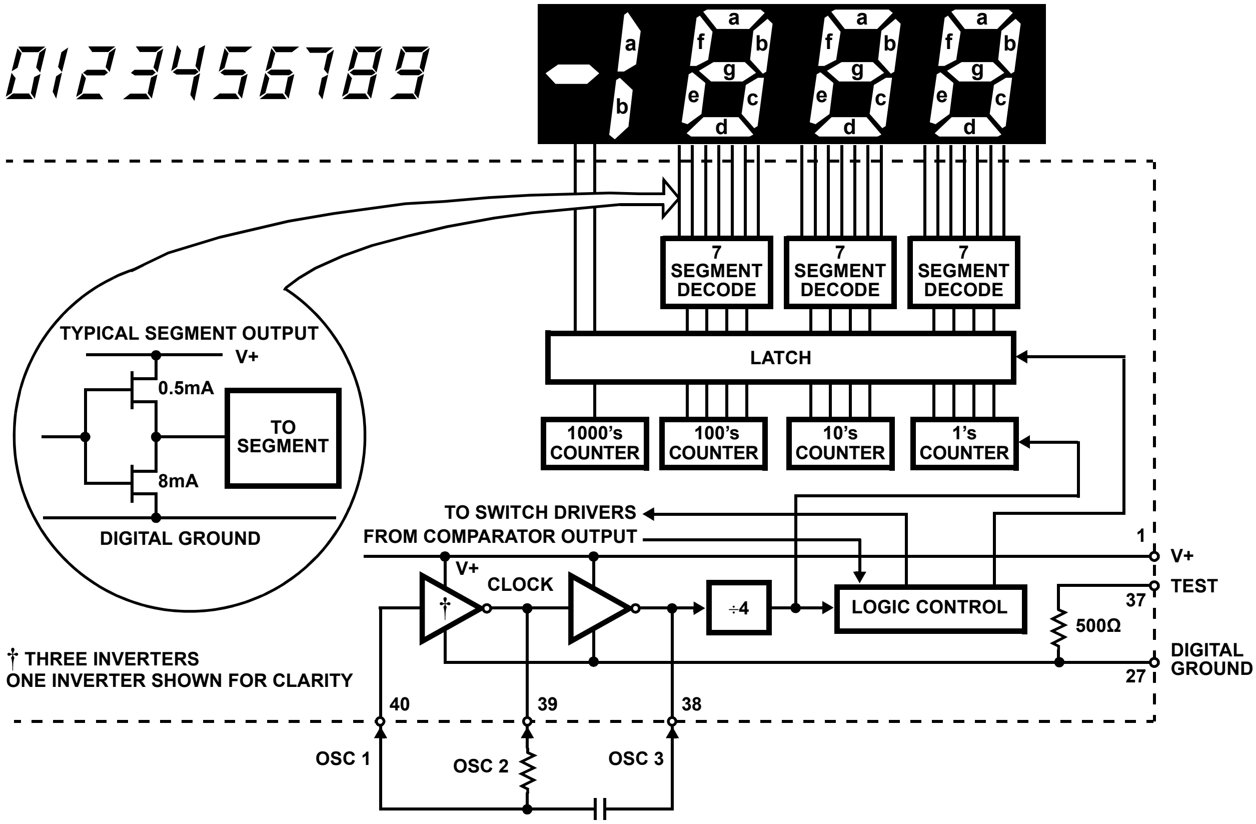


FIGURE 8. ICL7107 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the ICL7106 and ICL7107. Two basic clocking arrangements can be used:

1. Figure 9A. An external oscillator connected to pin 40.
2. Figure 9B. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference deintegrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^1/_3$kHz, etc., should be selected. For 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, $66^2/_3$kHz, 50kHz, 40kHz, etc., would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

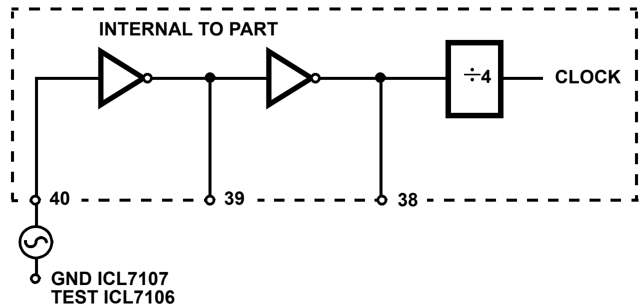


FIGURE 9A.

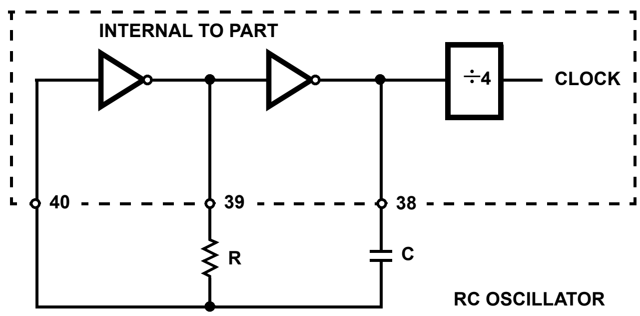


FIGURE 9B.

FIGURE 9. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 4µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.3V from either supply). In the ICL7106 or the ICL7107, when the analog COMMON is used as a reference, a nominal +2V full scale integrator swing is fine. For the ICL7107 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22µF and 0.10µF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47µF capacitor is recommended. On the 2V scale, a 0.047µF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1µF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent rollover error. Generally 1µF will hold the rollover error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected as shown in Equation 2:

$$f = \frac{0.45}{RC} \text{ For 48kHz Clock (3 Readings/sec),} \quad \text{(EQ. 2)}$$

$$C = 100pF.$$

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22µF. This makes the system slightly quieter and also avoids a divider network on the input. The ICL7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

ICL7107 Power Supplies

The ICL7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive IC. Figure 10 shows this application. See the ICL7660 datasheet for an alternative.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

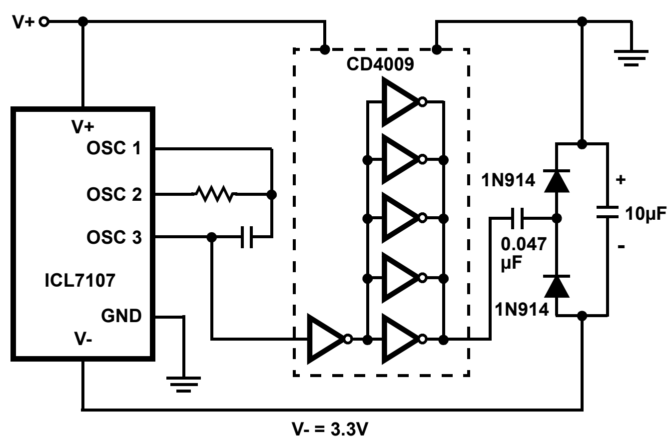


FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

Typical Applications

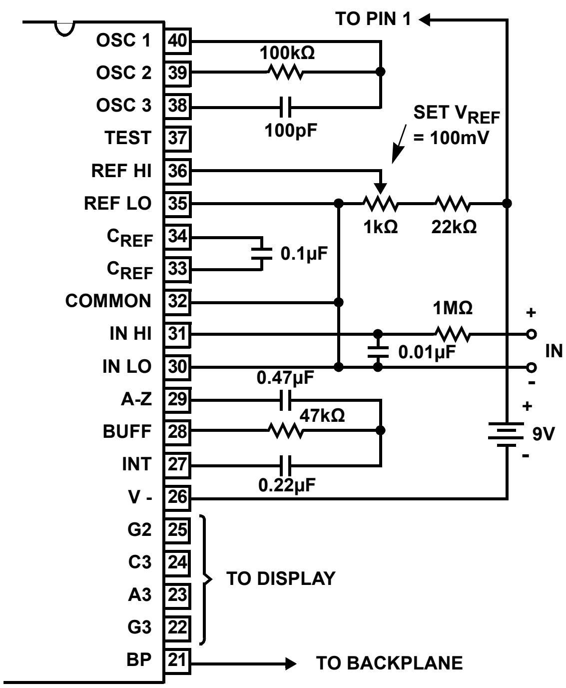
The ICL7106 and ICL7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

The following application notes contain very useful information on understanding and applying this part and are available from Intersil Corporation.

Application Notes

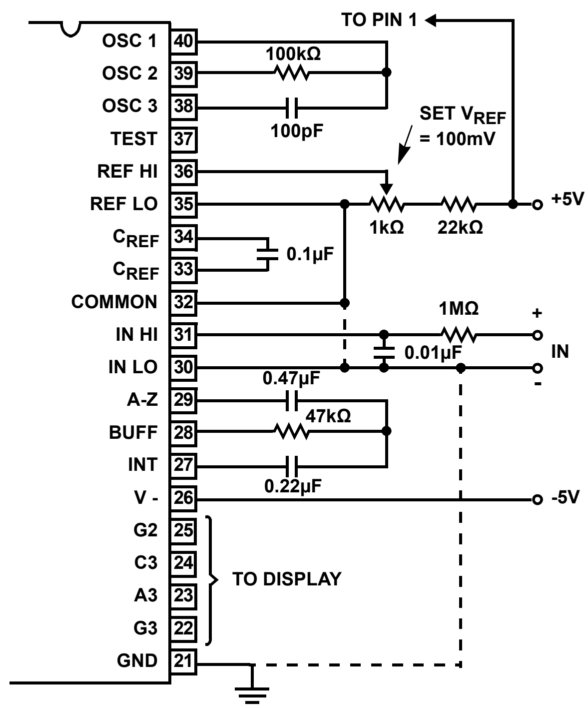
NOTE #	DESCRIPTION
AN016	"Selecting A/D Converters"
AN017	"The Integrating A/D Converter"
AN018	"Do's and Don'ts of Applying A/D Converters"
AN023	"Low Cost Digital Panel Meter Designs"
AN046	"Building a Battery-Operated Auto Ranging DVM with the ICL7106"
AN052	"Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"
AN9609	"Overcoming Common Mode Range Issues When Using Intersil Integrating Converters"

Typical Applications



Values shown are for 200mV full scale, 3 readings/sec., floating supply voltage (9V battery).

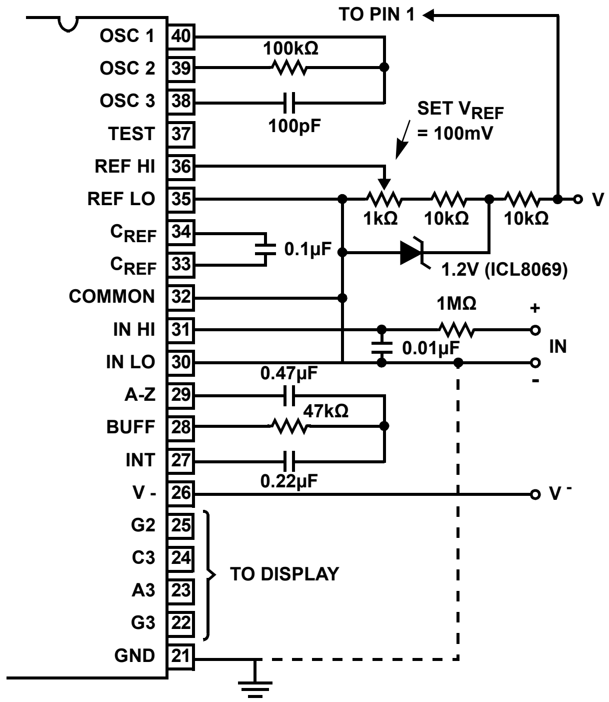
FIGURE 11. ICL7106 USING THE INTERNAL REFERENCE



Values shown are for 200mV full scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion in "Analog COMMON" on page 7.)

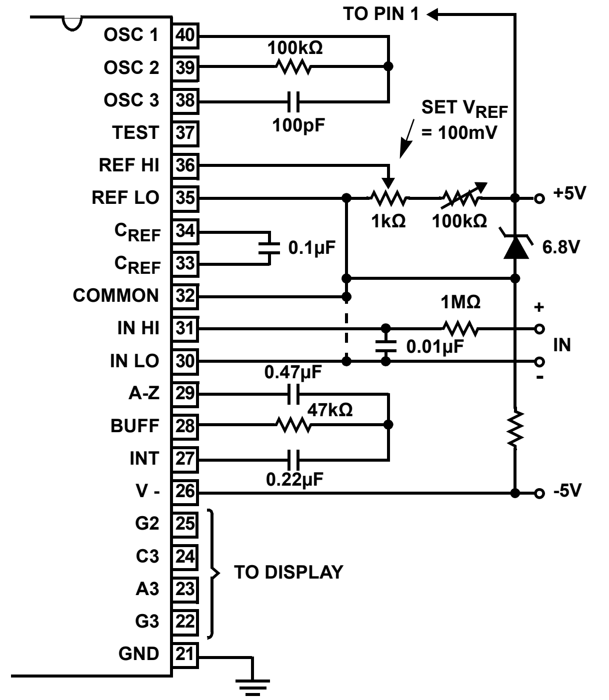
FIGURE 12. ICL7107 USING THE INTERNAL REFERENCE

Typical Applications (Continued)



IN LO is tied to supply COMMON establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply GND) and the preregulator is overridden.

FIGURE 13. ICL7107 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 12, IN LO may be tied to either COMMON or GND.

FIGURE 14. ICL7107 WITH ZENER DIODE REFERENCE

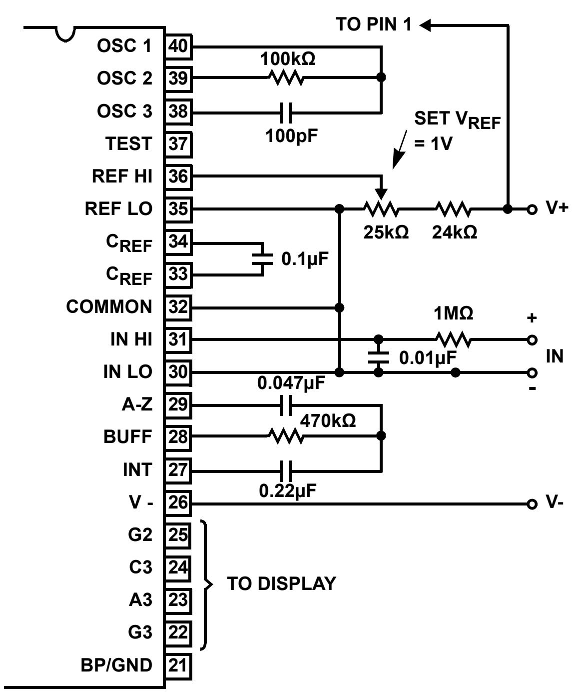
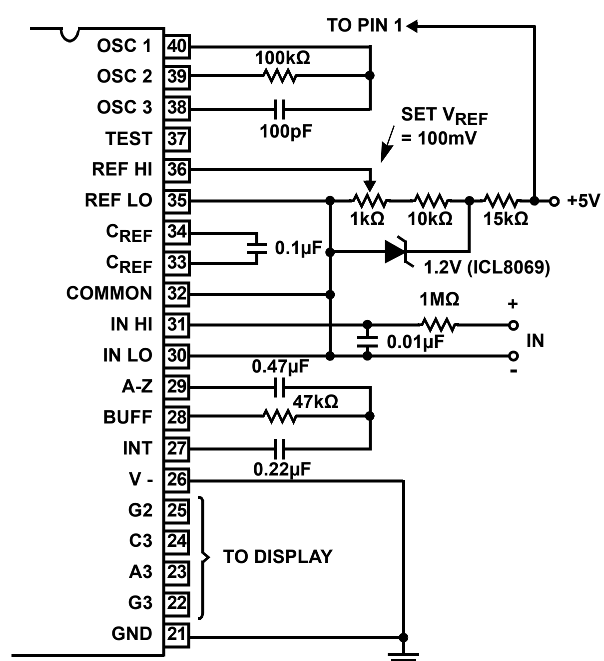


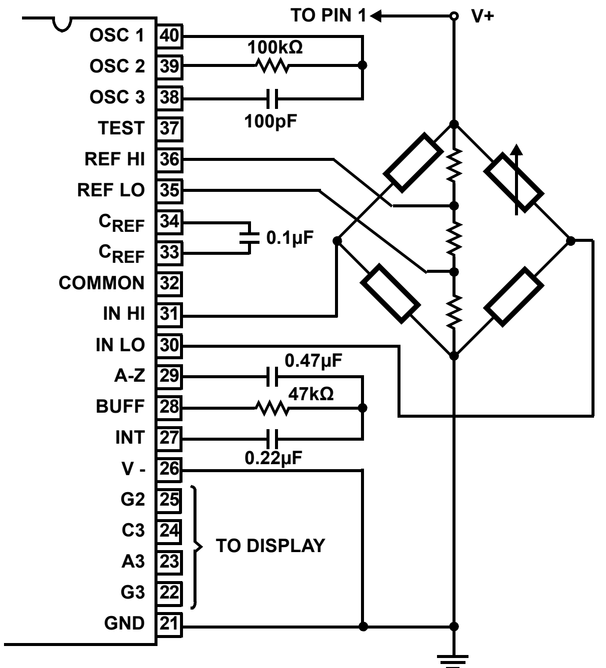
FIGURE 15. ICL7106 AND ICL7107: RECOMMENDED COMPONENT VALUES FOR 2V FULL SCALE



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

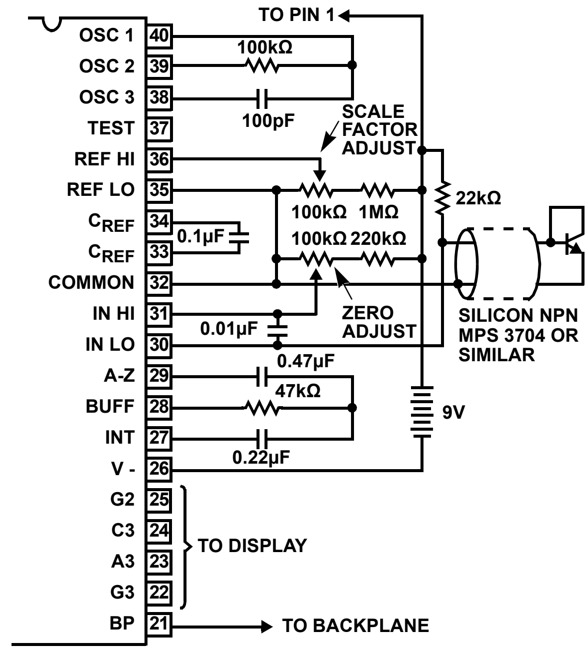
FIGURE 16. ICL7107 OPERATED FROM SINGLE +5V

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 17. ICL7107 MEASURING RATIOMETRIC VALUES OF QUAD LOAD CELL



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

FIGURE 18. ICL7106 USED AS A DIGITAL CENTIGRADE THERMOMETER

Typical Applications (Continued)

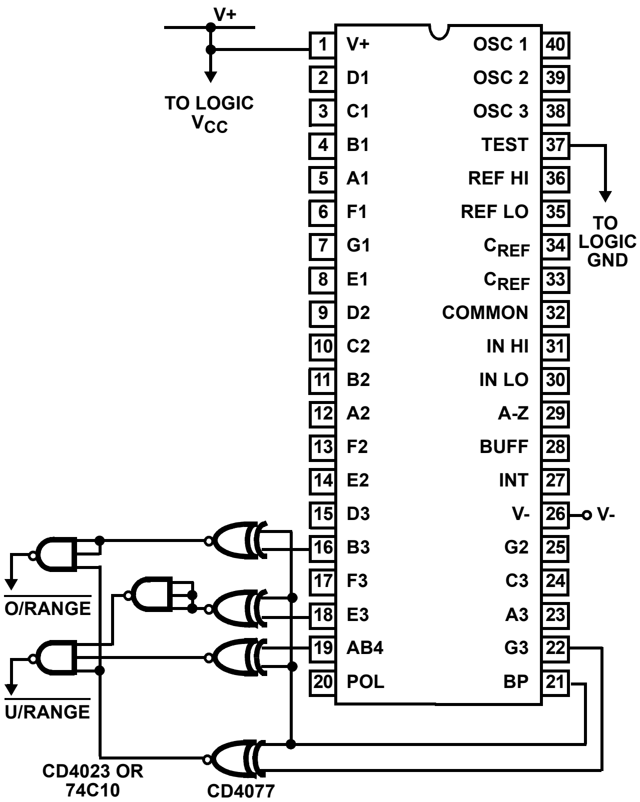


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNAL FROM ICL7106 OUTPUTS

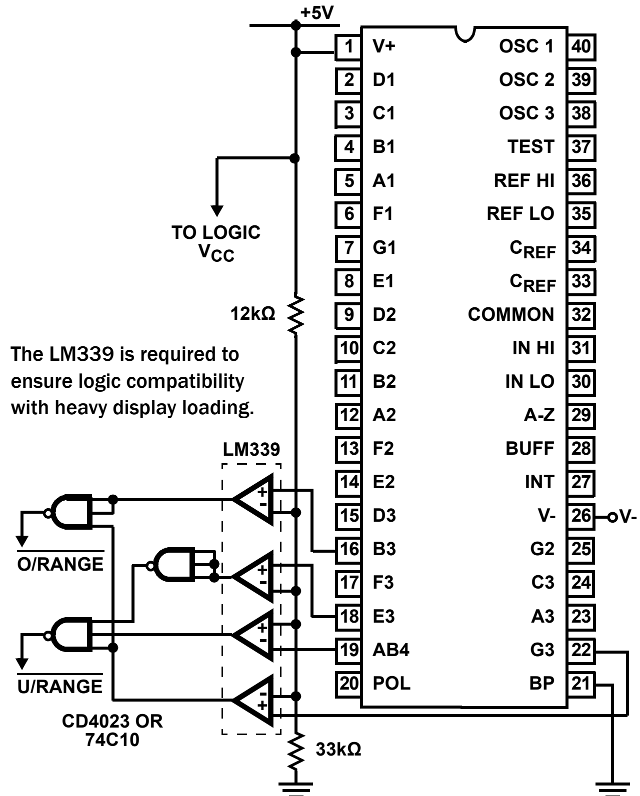
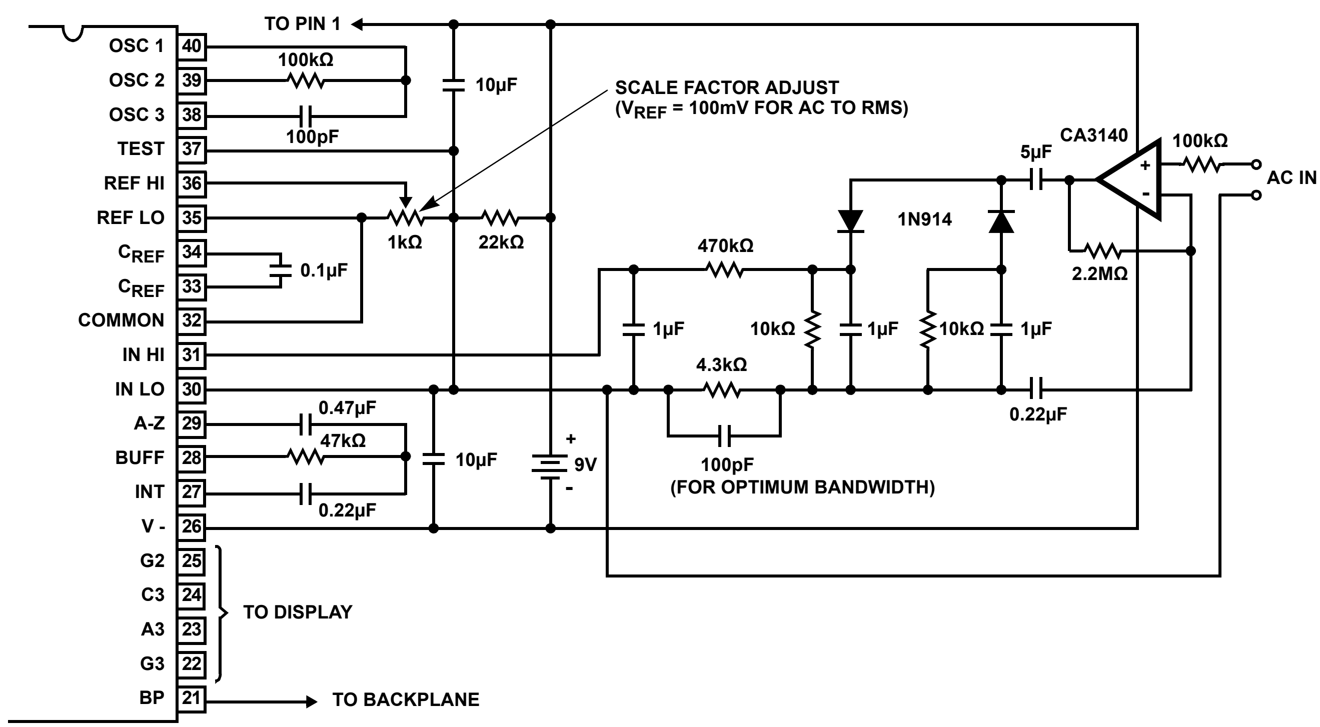


FIGURE 20. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM ICL7107 OUTPUT



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 21. AC TO DC CONVERTER WITH ICL7106

Typical Applications (Continued)

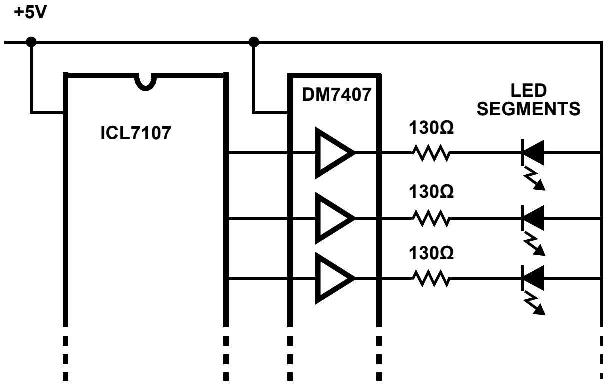


FIGURE 22. DISPLAY BUFFERING FOR INCREASED DRIVE CURRENT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 24, 2014	FN3082.9	Updated to the newest template. Page 1: Updated copyright area. Ordering Information table - removed all non Pb-free parts (all obsolete: ICL7106CPL, ICL7106CM44, ICL7107CPL, ICL7107RCPL, ICL7107RCPLZ, ICL7107SCPL, ICL7107CM44, ICL7107CM44T) and removed ICL7107RCPLZ (obsolete). Page 2, Removed the PDIP pinout for the ICL7107R, as it is obsolete. Page 4, Reworded Electrical Spec Note 9 (formerly note 5) from: "Not tested, guaranteed by design." to: "Limit is not production tested. The maximum was established via characterization and/or design simulations." Page 15, Added Revision History and About Intersil verbiage.

About Intersil

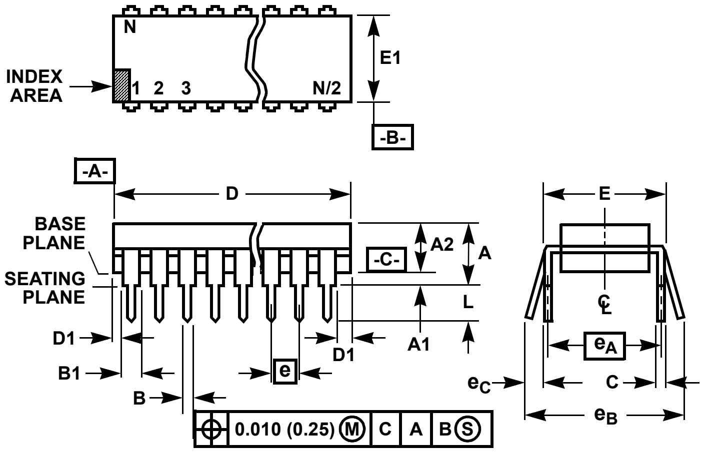
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Dual-In-Line Plastic Packages (PDIP)



NOTES:

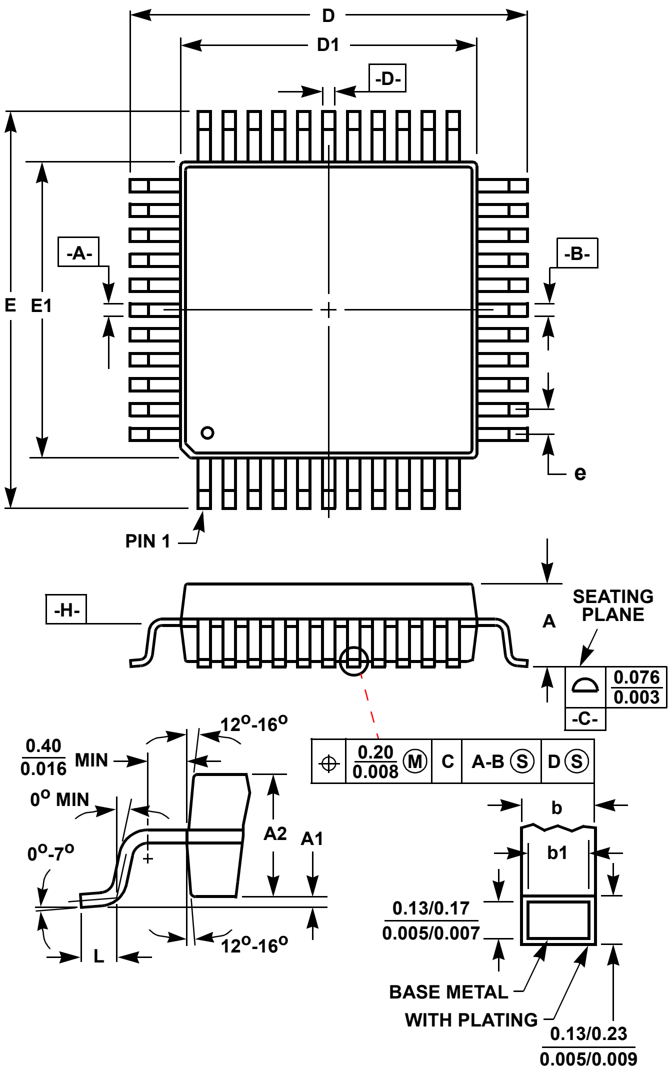
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 **(JEDEC MS-011-AC ISSUE B)**
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

Rev. 0 12/93

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C- .
4. Dimensions D1 and E1 to be determined at datum plane -H- .
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.